Fig. 1 is a sectional side view showing a prior art structure illustrating an integrated circuit structure on a silicon substrate with silicon dioxide spacers on the sidewalls of a polysilicon gate electrode.

Figs. 2A-2E schematically illustrate, in cross-sectional style, the key stages for fabricating a MOSFET device with silicon nitride spacers featuring a thin silicon oxide layer on the spacers to passivate the nitride during the salicide process.

Detailed Description of the Invention

This invention relates to a method and a semiconductor device prepared therefrom for passivation of a silicon nitride layer to prevent bridging between the gate and electrode and the source and drain regions of the transistor in a semiconductor device.

Fig. 2A is a cross-sectional view of the first stage of the process. A semiconductor substrate 11 is shown having isolation regions 12. The semiconductor substrate can be silicon or or an silicon on insulator (SOI) structure. The substrate 11 can be an N-type or P-type silicon. For illustrative purposes only, Fig. 2A shows semiconductor substrate as a single crystalline silicon is doped with a P-type dopant.

The isolation regions 12 may be shallow trench isolation (STI) regions or field oxide (FOX) regions that can be formed using any know localized oxidation of silicon (LOCOS) isolation methods. For example, thick field oxide (FOX) regions 12 can be formed by thermal oxidation in an oxygen-steam ambient at a temperature between 850° to 1050° C. The thickness of the regions is from about 4000 to about 6000 Å. Oxidation is prevented in the region between the FOX regions by using a patterned, oxidation resistant mask that is removed after the oxidation process is completed.

The gate electrode 15 comprises a dielectric layer 16 and a gate conductor layer 17. The gate dielectric layer 16 is formed on upper surface of substrate 11 between isolation regions 12. The gate electrode dielectric layer is typically silicon oxide, but it can also be silicon oxynitride or a high-K dielectric such as tantalum pentoxide (Ta_2O_5). The layer can also be a composite layer of silicon oxide and silicon nitride. The thickness of the gate dielectric is from about 20 to about 100 Å. The gate dielectric layer can be formed by using conventional chemical vapor deposition (CVD) techniques.